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FIG. 1

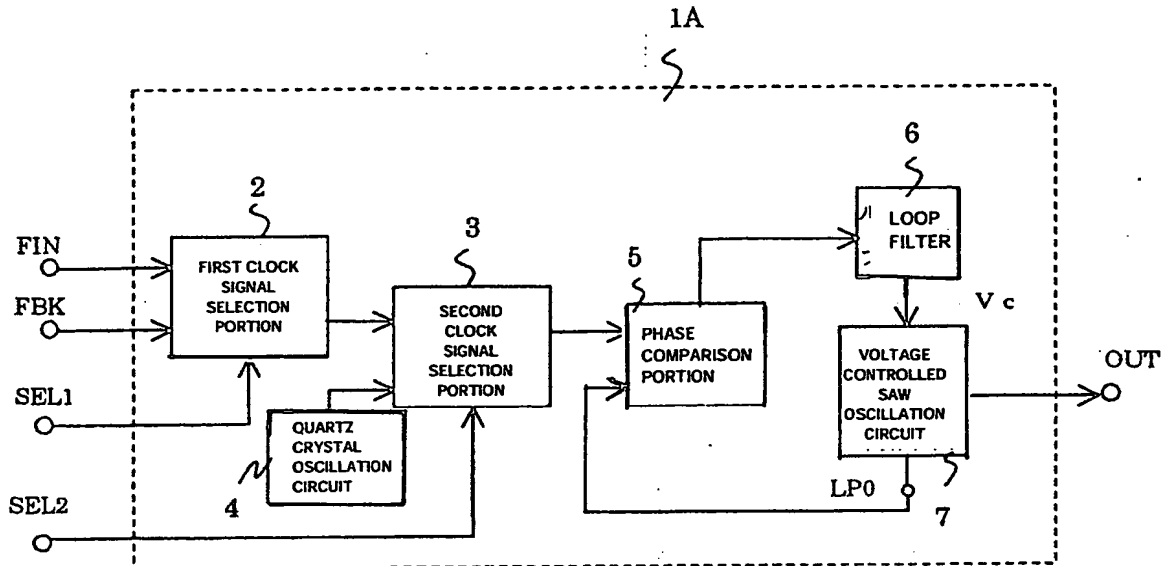


FIG. 2

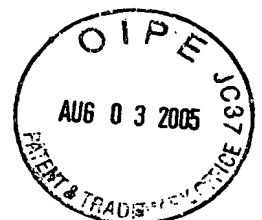
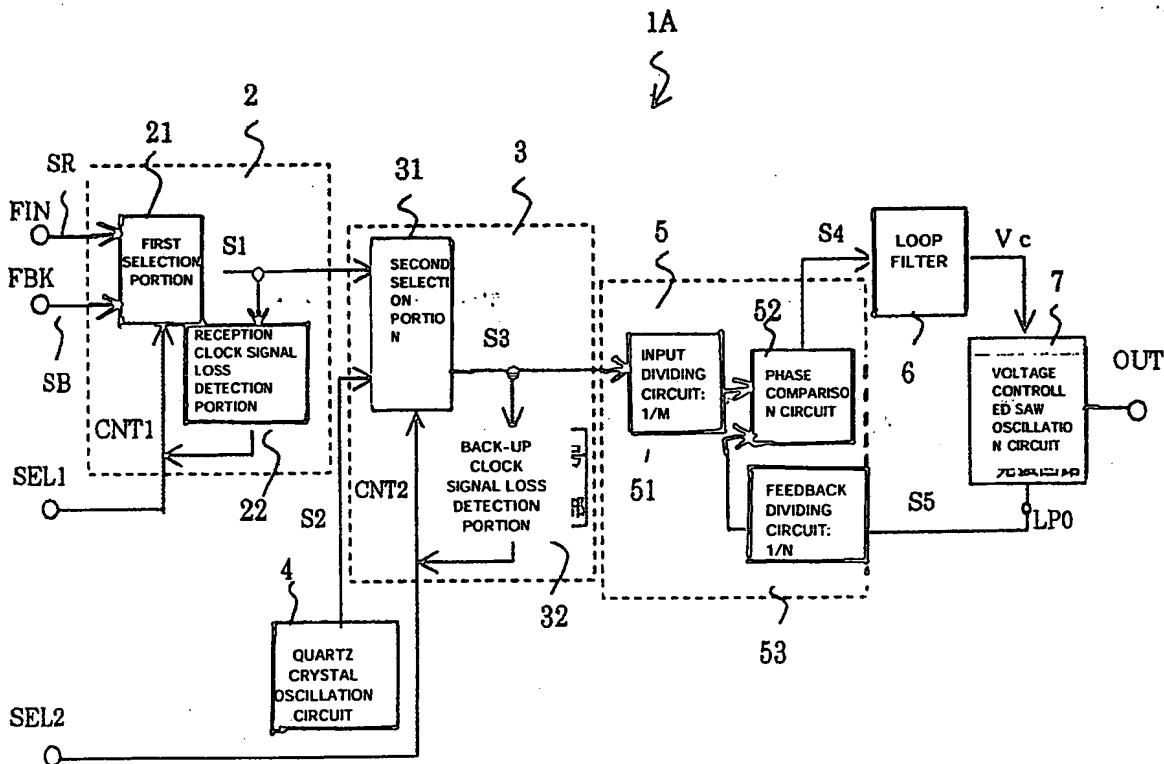
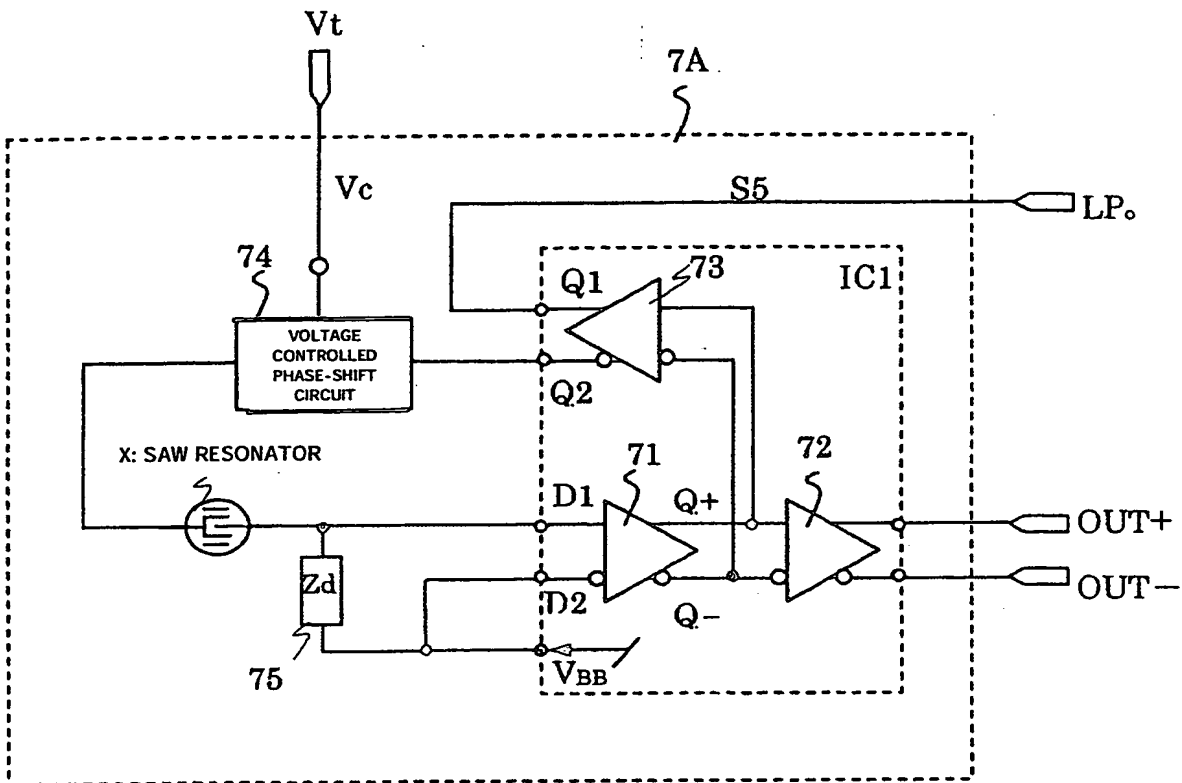


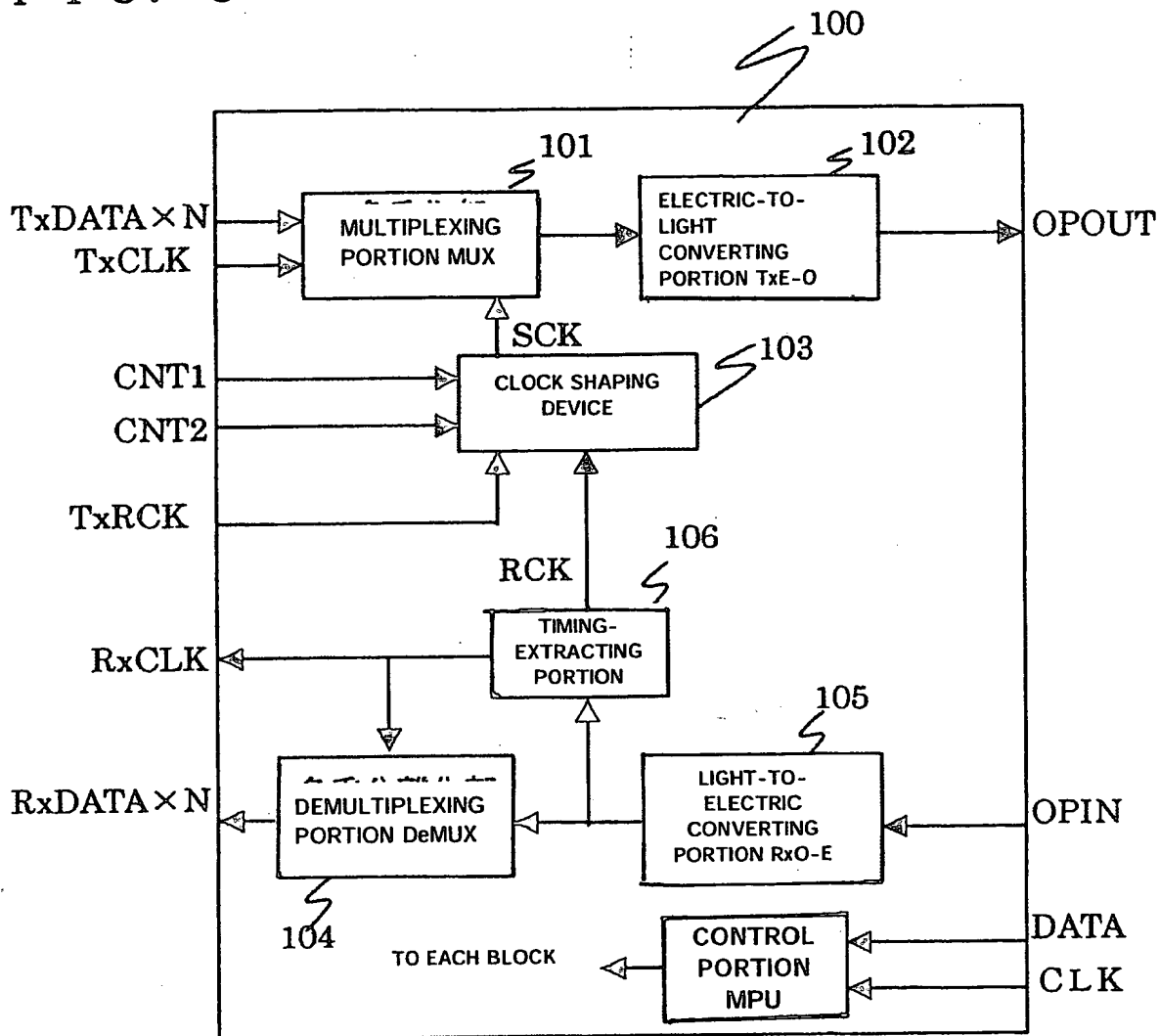
FIG. 3



The diagram illustrates a PLL system with a multi-output divider. The main PLL loop includes a quartz crystal oscillator circuit (4) providing a reference signal to a first selection portion (21) and a reception clock signal loss detection portion (22). The first selection portion (21) also receives feedback signals (SR, FBK, SB) and a control signal (CNT1). Its output goes to a second selection portion (31), which also receives a control signal (CNT2). The second selection portion (31) outputs to an input dividing circuit (51) with a division ratio of 1/M. This circuit is part of a larger block (5) that also contains a phase comparison circuit (52) and a feedback dividing circuit (53) with a division ratio of 1/N. The phase comparison circuit (52) receives a signal from the input dividing circuit (51) and the feedback dividing circuit (53). The output of the phase comparison circuit (52) goes to a loop filter (6). The loop filter (6) outputs a control voltage (Vc) to the first selection portion (21) and the second selection portion (31). The output of the loop filter (6) also goes to a multi-output divider (7B). This divider (7B) contains a voltage controlled phase-shift circuit (74) driven by Vc, which is connected to a SAW resonator (X). The output of the phase-shift circuit (74) goes to a series of inverters (77, 78, 79-1, 79-2, ..., 79-n) connected in a chain. The outputs of these inverters are labeled OUT1, OUT2, ..., OUTn (LPn). The divider (7B) also receives a control signal (Vt) and provides a feedback signal (Vc) to the main PLL loop.

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FIG. 6



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FIG. 7
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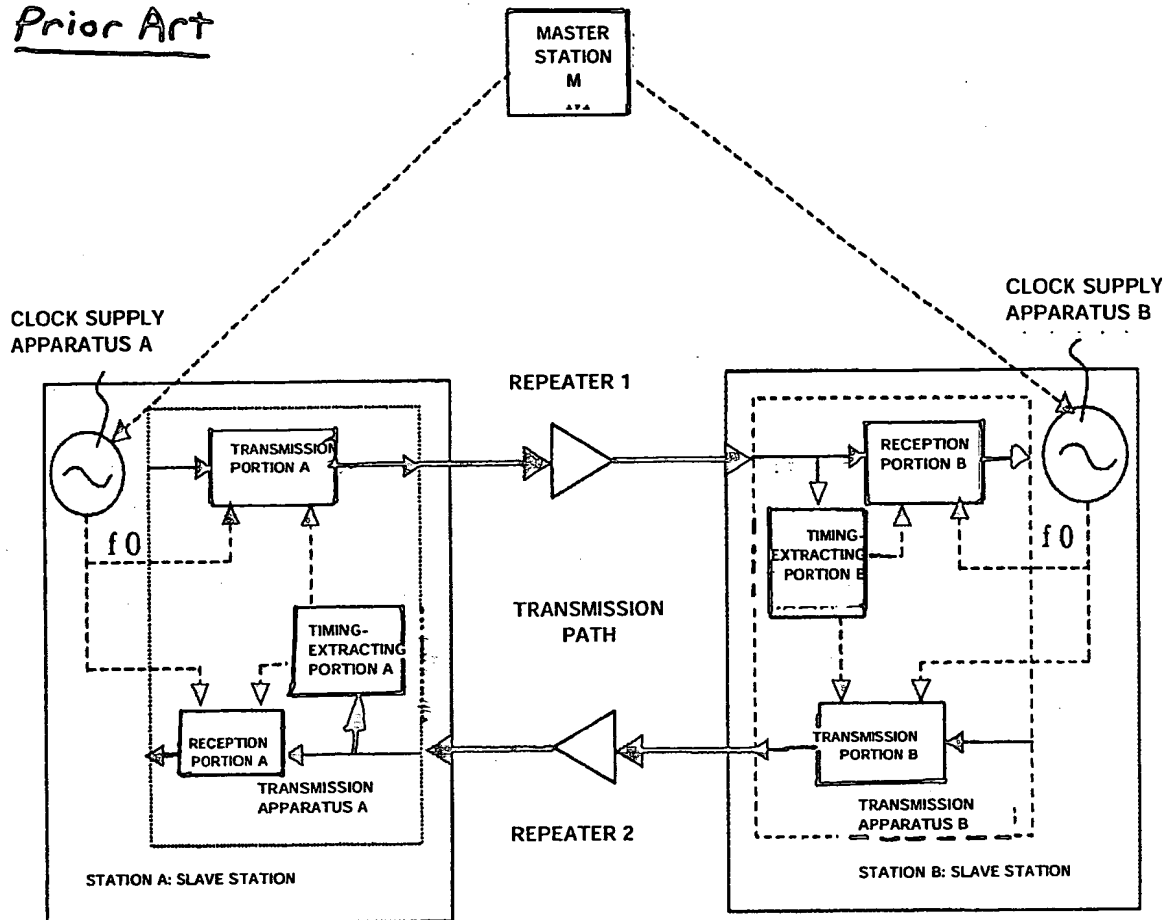
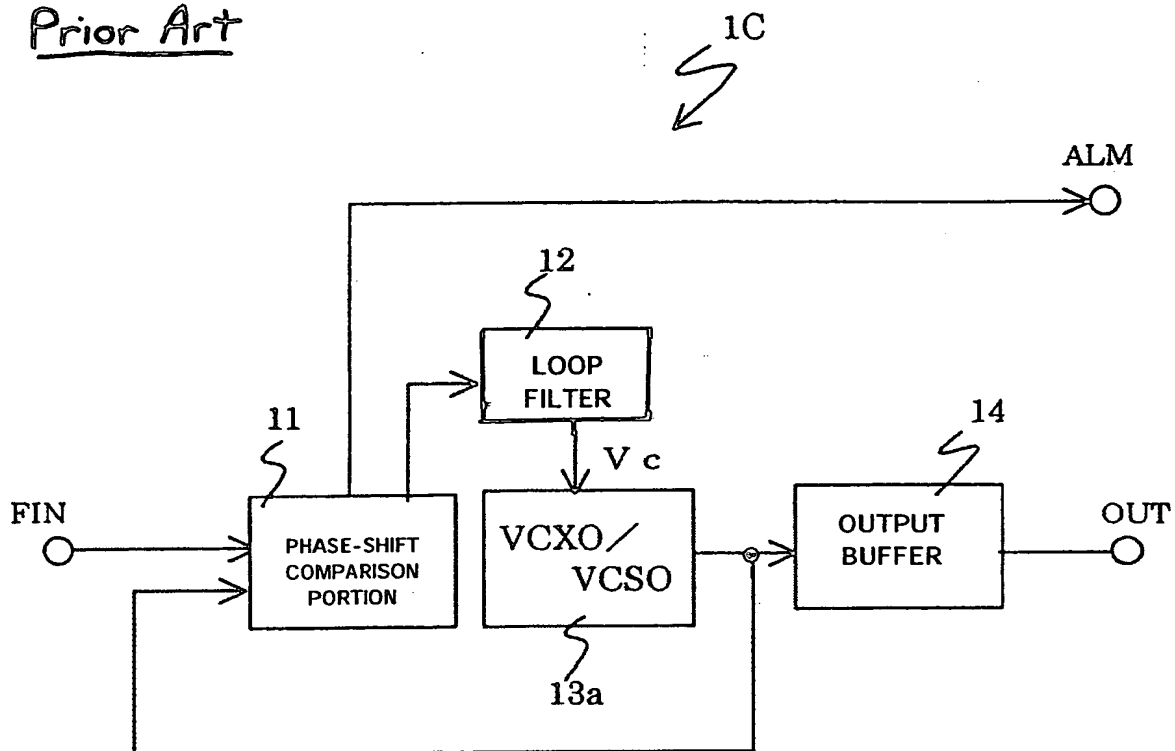


FIG. 8
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FIG. 9
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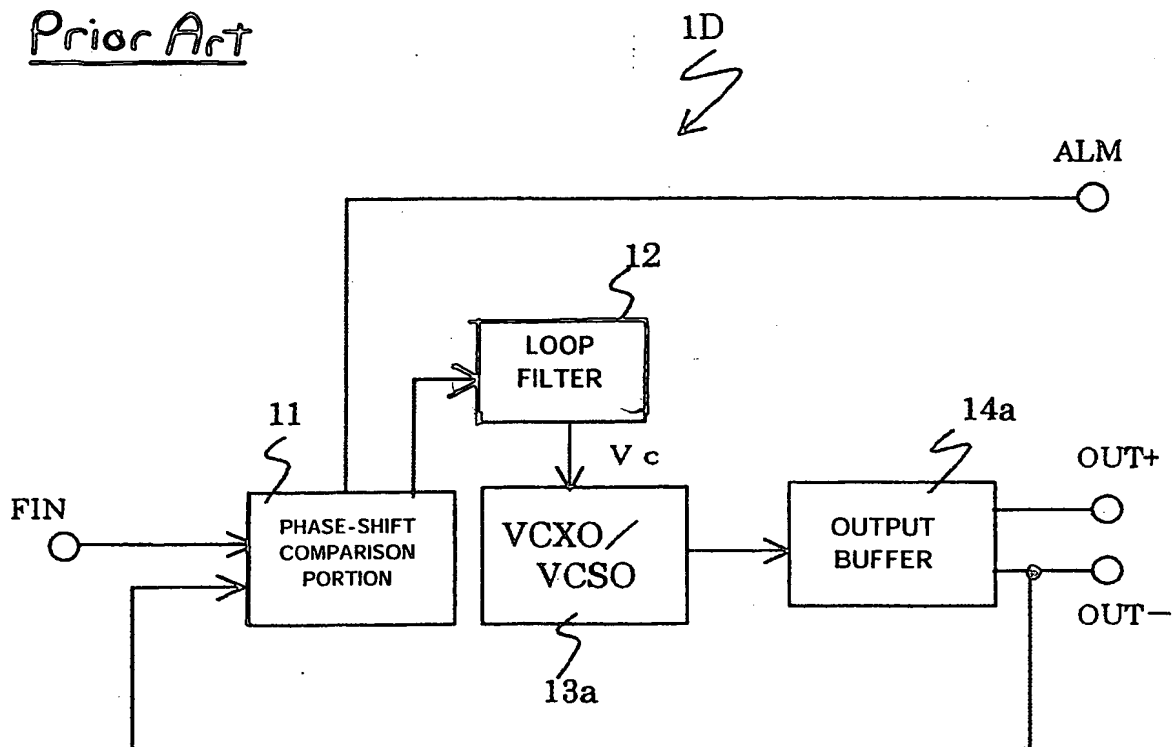


FIG. 10
Prior Art

